

## REMARKS

Claims 1-12 were pending in the above-identified application when last examined and are amended as indicated above. The claim amendments clarify the claim language and are not intended to limit the scope of the claims, unless the claim language is expressly quoted in the following remarks to distinguish over the art cited.

Claims 3 and 6-8 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claim 7 is canceled.

In regard to claim 3, the Examiner on page 2 of the Office Action indicated that use of the term “**the**” in “**the** first portion of the first operand signal” recited in the last six lines of claim 3 was not the same as the preceding recitation of “a first portion of the first operand signal” because “the width of the first/second portion are different.” Applicant respectfully traverses the rejection. Even in a case where the data width of a signal applied to a multiplier in the first mode differs from the data width of a signal applied to the multiplier in the second mode, a portion can still be selected that is common to both modes. Accordingly, use of “**the**” in the second reference of the portion is correct.

Claim 6 is amended to replace “second partial multiplicand” with “fourth partial multiplicand” as the Examiner suggested. Claim 8 is also believed to be clear and definite in view of the amendment to claim 6.

In view of the above remarks and amendments, Applicant requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

Claim 10 was rejected under 35 U.S.C. § 102(b) as anticipated by any one of U.S. Patent No. 5,751,622 (Purcell), U.S. Patent No. 5,586,070 (Purcell), and U.S. Patent No. 6,286,024 (Yano et al.). Claim 10 is canceled.

Claims 1-2, 4-9, and 11 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,764,558 (Pearson). Claims 1 and 7 are canceled. Applicant respectfully traverses the rejection of claims 2, 4-6, 8, 9, and 11.

Claim 2 is amended to depend from claim 3, which was objected to but is now in condition for allowance for the reasons given below. Claim 2 is thus believed patentable over Pearson for at least the same reasons that claim 3 is patentable over Pearson.

Independent claim 4 as amended distinguishes over Pearson at least by reciting, “a first two’s complement unit and a second two’s complement unit that respectively receive a first input value and a second input value and that respectively output a first multiplicand and a second multiplicand, wherein the first and second multiplicands respectively represent absolute values of the first and second input values for signed multiplication in the second mode; and operand selection logic coupled to the multipliers and the first and second two’s complement units, wherein the operand selects parts of the first and second multiplicands that are respectively input to the first, second, third, and fourth multipliers.”

In accordance with an aspect of the invention, two’s complement units can determine absolute values of input values before a multiplying unit multiplies the absolute values. The sign of the resulting product can then be corrected according to the original signs of the multiplicands. In contrast, the abstract of Pearson describes, “In response to the data processing system being operated in a signed mode, selected bits in selected partial products in selected multipliers are complemented, and  $2^B$  is added to a selected intermediate result so that when the intermediate results are appropriately weighted and added together, a result that is the product of two operands having  $2B$ -bits may be calculated.” Pearson thus complements partial products, but Pearson fails to disclose or suggest two’s complement units that respectively output a first multiplicand and a second multiplicand.

Claim 4 and claims 5, 6, 8, and 9, which depend from claim 4, are thus believed patentable over Pearson.

Claim 11 is amended to depend from claim 12, which was objected to but is now in condition for allowance for the reasons provided below. Claim 11 is believed patentable over Pearson for at least the same reasons that claim 12 is patentable over Pearson.

For the above reasons, Applicant requests reconsideration and withdrawal of this rejection under 35 U.S.C. § 103.

Claims 1-2, 4-9, and 11 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,286,024 (Yano et al.) Claims 1 and 7 are canceled. Applicant respectfully traverses the rejection of 2, 4-6, 8, 9, and 11.

Claim 2 is amended to depend from claim 3, which was objected to but is now in condition for allowance for the reasons provided below. Claim 2 is believed patentable over Yano for at least the same reasons that claim 3 is patentable over Yano.

Independent claim 4 as amended distinguishes over Yano at least by reciting, “a first two’s complement unit and a second two’s complement unit that respectively receive a first input value and a second input value and that respectively output a first multiplicand and a second multiplicand, wherein the first and second multiplicands respectively represent absolute values of the first and second input values for signed multiplication in the second mode; and operand selection logic coupled to the multipliers and the first and second two’s complement units, wherein the operand selects parts of the first and second multiplicands that are respectively input to the first, second, third, and fourth multipliers.”

Yano fails to disclose or suggest the use of two’s complement units on input values as recited in claim 4. For example, beginning at column 9, line 16, Yano describes, “At that time, according to Eq.(A), it is to be noted that both the multiplicand and the multiplicator must be handled as unsigned data in Z1, the multiplicand and the multiplicator must be handled as unsigned data and signed data (display data of two's complement) respectively in Z2, the multiplicand and the multiplicator must be handled as signed data and unsigned data respectively in Z3, and both the multiplicand and the multiplicator must be handled as signed data in Z4.” Yano thus describes techniques involving signed and unsigned multiplications, but fails to disclose or suggest two’s complement units meeting the recited restrictions in claim 2.

Claim 4 and claims 5, 6, 8, and 9, which depend from claim 4, are thus believed patentable over Yano.

Claim 11 is amended to depend from claim 12, which was objected to but is now in condition for allowance for the reasons provided below. Claim 11 is believed patentable over Yano for at least the same reasons that claim 12 is patentable over Yano.

For the above reasons, Applicant requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103.

Claims 3 and 12 were objected to as dependent upon a rejected claim but were indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 3 is amended to independent form including the limitations of canceled base claim 1. Claim 12 is amended to independent form including the limitations of canceled base claim 10. In view of the above amendments, Applicant requests reconsideration and withdrawal of the objection to claims 3 and 12.

In summary, claims 1-12 were pending in the application. This response amends claims 2-4, 6, 8, 11, and 12 and cancels claims 1, 7, and 10. For the above reasons, Applicant respectfully requests allowance of the application including claims 2-6, 8, 9, 11, and 12.

Please contact the undersigned attorney at (408) 927-6700 if there are any questions concerning the application or this document.

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Respectfully submitted,



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